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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech I Year II Semester Regular & Supplementary Examinations October-2022

DIGITAL LOGIC DESIGN

(Common to CSE, CSIT & CCC)

Time: 3 hours

Max. Marks: 60

(Answer all Five Units 5 x 12 = 60 Marks)

UNIT-I

- 1 a Represent the decimal number 3451 in L1 6M
 i)BCD
 ii)Hexadecimal and
 iii)perform $(-60)-(-20)$ in binary using the signed-2's complement
- b Simplify the Boolean expressions to minimum number of literals L2 6M
 i) $(A + B)(A + C')(B' + C')$
 ii) $AB + (AC)' + AB'C(AB + C)$

OR

- 2 a Explain the Excess-3 code. L2 6M
 b Simplify the Boolean expressions to minimum number of literals L5 6M
 i) $X' + XY + XZ' + XYZ'$ ii) $(X+Y)(X+Y')$

UNIT-II

- 3 a Simplify the Boolean expression using K-map and implement using NAND gates L5 6M
 $F(A,B,C,D) = \sum m(0,2,3,8,10,11,12,14)$
 b Design the circuit by Using NOR gates $F = (X+Y).(X'+Y'+Z')$ L5 6M
- OR**
- 4 a Design the circuit by Using NAND gates $F = ABC' + DE + AB'D'$ L5 6M
 b Explain NAND- NOR implementations. L2 6M

UNIT-III

- 5 a Explain about parallel Adder. L2 6M
 b Implement the following Boolean function using 8:1 multiplexer L5 6M
 $F(A,B,C,D) = \sum \circ (0,1,2,5,7,8,9,14,15)$

OR

- 6 a Explain Design Procedure of combinational circuits. L2 6M
 b Explain Full binary subtractor in detail. L2 6M

UNIT-IV

- 7 a Explain the Logic diagram of RS flip-flop. L2 6M
 b Explain about Ring counter. L2 6M

OR

- 8 a Write difference between Combinational and Sequential circuits. L5 6M
 b Draw and explain the operation of T Flip-Flop. L5 6M

UNIT-V

- 9 a Compare between PROM, PLA & PAL. L2 6M
 b Encode the 11-bit code 10111011101 into 15 bit information code. L5 6M

OR

- 10 a Explain the memory decoding, error detection and correction. L1 6M
 b Implement the following function using PLA L5 6M
 $A(x,y,z) = \sum m(1,2,4,6)$ $B(x,y,z) = \sum m(0,1,6,7)$ $C(x,y,z) = \sum m(2,6)$

*** END ***